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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,063	06/24/2003	Joseph B. Allen	BUR920030034US1	1062

30449 7590 02/06/2007

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EXAMINER	
LIEW, ALEX KOK SOON	
ART UNIT	**PAPER NUMBER**
2624	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/604,063	ALLEN ET AL.	
	Examiner	Art Unit	
	Alex Liew	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The amendment filed on 11/27/06 is entered and made of record.

Response to Applicant's Arguments

1. The applicant states on page 10 – 11: [In addition, the examiner's statement that "the template shown in fig 3 has an inner and outer region error boundary" adds further ambiguity to the examiner's identification of "the template" because in fig 3 of Fridge, both inner template 62 and outer template 64 have only outer boundaries and do not have any inner boundaries.]

The limitation: forming a first shape pattern is shown in column 5 lines 47 – 52 of Fridge and figure 3, where the first formed shape is read as the combination inner and outer boundary.

2. The applicant states on page 11 – 12: [In response, Applicants respectfully contend that the examiner's argument is incorrect. Since the examiner alleges that the conductive layer 70 on Fig 4 of Fridge represents the second shape pattern, Applicants maintain that the second shape pattern does not include the first shape pattern. If the examiner considers the inner template 62 to represent the first shape pattern, then it is clear from Fig 4 of Fridge that the conductive layer 70 does not include the inner template 72, because a portion of the inner template 72 is external to the conductive layer 70.]

The limitation: forming a second shape pattern, said second shape pattern including the first shape pattern and error shapes is shown in col. 6 lines 17 – 24 and figure 4, where the second shape *includes* the all of the area of the inner template and part of the area of the outer template. The applicant did not specifically claim how the first pattern shape is *included* in the second shape, whether the first shape is all inside in second shape or partially inside the second shape. The second forming shape also includes error shapes shown in fig 4 – 74 and 76.

3. The applicant states on page 12: [However, Fridge does not disclose that the region 74 and the excess area 76 are extracted from the second shape pattern.]
The applicant did not specifically claim whether the error shape, 4 – 74, is within the inner template, which the area of the first and second forming shape.

4. The applicant states on page 13: [In response, Applicants respectfully content that the shapes 172 and 174 in Fig. 6 of Fridge are not derived from any error shapes (as required by claims 1 and 16) but rather are regular circuit board areas, as disclosed in Fridge, col. 9 lines 17-20.]
The examiner disagrees. Figure 4 – 74 is read as error shapes, where the void defect are defects on the print circuit board.

5. The applicant states on page 14: [In response, Applicant respectfully contends that although Chung discloses deleting shapes, Chung does not disclose deleting

shapes such that only unique environment shapes satisfying a selection criterion remain.]

The criterion is shown in fig 8 with MIN value, where the minimum value is determined analytically by inspection (see col. 9 lines 27 – 32). The criterion, MIN, is chosen based on the 'environment' of the pattern of the inspection substrate.

6. The applicant states on page 15: [In response, Applicant respectfully contend that even if Fridge discloses grouping according to the doses, Fridge does not disclose grouping to "a combination of an area of error shape and a smallest linear dimension of the error shape" as required by claim 4 and 19.]

The examiner agrees with the applicant, and will withdraw the rejection. However, in the examiner's search, Brecher (US pat no 5,544,256) discloses grouping to a combination of an area of error shape and a smallest linear dimension of the error shape (see fig 7 and col. 10 lines 3 – 5 – the circle shape defect is the smallest defect and is grouped with other shape errors). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include grouping to a combination of an area of error shape and a smallest linear dimension of the error shape because the smallest error shape are almost insignificant, so the grouping those smallest error shape with other shape groups save processing due to having to process less error shapes.

7. The applicant states on page 15: [In addition with respect to claims5 and 20, Applicants respectfully contend that Fridge in view of Chung does not teach or suggest the feature: "expanding each error shape in the subset to form a corresponding expanded shape; and form the at least one environment shape corresponding to each expanded shape by removing all portions of the expanded shape which are common to the second shape pattern."]

The examiner agrees with the applicant that either Fridge or Chung does not disclose expanding shape step, as shown in figure 5 – 66 of the current claimed invention. However, in the examiner's new search shows Bishop (US pat no 4,589,140) discloses expanding each error shape in the subset to form a corresponding expanded shape (see fig 7b – the defect shape is magnified or expanded) and form the at least one environment shape corresponding to each expanded shape by removing all portions of the expanded shape which are common to the second shape pattern (fig 7b is the environment shape; also the rest of the image, other than the defect area, in fig 7c are remove from to obtain the image in fig 7b). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include expanding the area of the defect because to obtain the detail shape of the defect in order to classify the defect, so it can be use later to identify defect shapes similar to the one being identify currently.

8. The applicant states, on page 16: [In addition with respect to claims 12 and 27, Applicants respectfully contend that Fridge in view of Chung does no teach or suggest

the feature: "wherein the N independent characteristic comprise at least two of: the vertex count of the environment shape, the area of the environment shape, and a perimeter of the environmental shape"]. The examiner disagrees with the applicant. Chung discloses vertex count of the environment shape (see fig 8 – 802 – the number of shape count must be produce in order to perform the condition test and see fig 8 – 814 – at some point during the operation, at least one of the shapes will reached it maximum number of shape counts, which will satisfies the condition in 814) and the dimensions of the shape areas (see col. 1 lines 57 – 61 – the common shapes of defects disclosed by Chung are rectangles and col. 8 lines 47 – 48 – the dimensions of the defects are shown, from these dimensions one can obtain the perimeter and area values).

9. The applicant states on page 17: [Therefore Applicants respectfully request that the Examiner supply evidence to support the Examiner's use of official notice in alleging that "it is well known in the art for one kill in the art to use XOR function to extract errors shapes."] Morrin (US pat no 4,005,411) discloses obtaining a correlated error image by using exclusive OR operator (see col. 3 lines 66 – 67 to col. 4 lines 1 – 2).

10. The applicant states on page 18: [The examiner has not stated and motivation for modifying Fridge by the alleged teaching of Chung with respect to the preceding feature of claims 14 and 29.] The examiner asks the applicant to see the motivation provided in claim 1. In addition, one skill in the art would add additional shapes onto the an

environment with similar shapes is because to ease classification methods when all of the similar shapes are around in the same areas, improving productivity and efficient during semiconductor inspection process.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 3, 11, 12, 14, 16 – 18, 26, 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fridge (US pat no 4,648,053) in view of Chung (US pat no 5,481,472).

With regards to claim 1, Fridge discloses a method for reducing a number of shapes, said method comprising the steps of:

- forming a first shape pattern (column 5 lines 47 – 52 and figure 3, where the first formed shape is read as the combination inner and outer boundary),
- forming a second shape pattern, said second shape pattern including the first shape pattern and error shapes (forming a second shape pattern, said second shape pattern including the first shape pattern and error shapes is shown in col.

6 lines 17 – 24 and figure 4, where the second shape *includes* the all of the area of the inner template and part of the area of the outer template),

- extracting the error shapes from the second shape pattern (see col. 6 lines 20 – 32 – the excess area is read as the error shapes as shown in fig 4 – 74 and 76),
- deriving from a subset of the error shapes at least one environment shape corresponding to each error shape in the subset of the error shapes, said environment shape reflecting a local geometric environment of its corresponding error shape (see col. 4 lines 17 – 23 – the defects is enlarged for inspection, see fig 5 – where each component 172, 174, 176, and 178 – the enlarged image is read as the environment shape, which includes error shapes also enlarged).

But fails to disclose deleting a subset of the environment shapes such that only unique environment shapes satisfying a selection criterion remain. Chung discloses deleting a subset of the environment shapes such that only unique environment shapes satisfying a selection criterion remain (see col. 11 lines 15 – 19 – the list contains information about shapes, see col. 1 lines 8 – 13, 50 – 55, some are removed and some are appended, the criterion is shown in fig 8 with MIN value and see col. 13 lines 1 – 5 as an example). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include deleting a subset of the environment shapes because the number of data operated on during analysis for displacements is very much reduced and can be accomplished at very high speed (see col. 12 lines 11 – 17).

With regards with claim 2, Fridge discloses all of the claim elements / features as discussed above in rejection for claim 1 and incorporated herein by reference, but fails to disclose wherein the subset of the error shapes is a first group of the at least one group. Chung discloses a method of claim 1, said method further comprising distributing the error shapes into at least one group such that the at least one group is defined by a grouping criterion (see fig 19 –having assigned doses 25, 26 and 27, groupings of shapes, corresponding to different group of shapes, col. 13 lines 25 – 30, also see fig 10 – on the 'X-Coord' column it specify the position, x and y coordinate, the width and height, dose – col. 1 lines 50 – 55, and an identification code, see col. 6 lines 27 – 37), wherein the subset of the error shapes is a first group of the at least one group. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include subset of the error shapes because to organize each shape into each categories for classification purposes, so the system is able to identify which error shapes are most common in a semi-conductor chip pattern.

With regards to claim 3, see the rejection and rationale for claim 2.

With regards to claim 11, Fridge discloses all of the claim elements / features as discussed above in rejection for claim 1 and incorporated herein by reference, but fails to disclose selection criterion relates to N independent characteristics. Chung discloses a method of claim 1, wherein the selection criterion relates to N independent characteristics of each environment shape such that N is at least 1 (see col. 1 lines 50 –

55 – there are four characteristic present, position of the shape x and y coordinate, and height and width; h and w), and wherein the deleting step includes sorting the environment shapes in accordance with N sort keys such that the N sort keys are the N independent characteristics (see code delta is sorted in order of the position). It would have been obvious to one having ordinary skill in the art at the time of the invention to include each shape having N characteristic present because to organize each shape into each categories for classification purposes, so the system is able to identify which error shapes are most common in a semi-conductor chip pattern.

With regards to claim 12, see the rejection for claim 11. Also see response to applicant's section.

With regards to claim 14, see the rejection and rationale for claim 1 (citation for last limitation – Chung col. 11 lines 15 – 19 – removal and appended).

With regards to claim 16, see the rejection and rationale for claim 1

With regards to claim 17, see the rejection and rationale for claim 2

With regards to claim 18, see the rejection and rationale for claim 3

With regards to claim 26, see the rejection and rationale for claim 11.

With regards to claim 27, see the rejection and rationale for claim 12.

With regards to claim 29, see the rejection and rationale for claim 14.

3. Claims 4 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fridge (US pat no 4,648,053) in view of Chung (US pat no 5,481,472) as applied to claim 3 further in view of Brecher (US pat no 5,544,256).

With regards with claim 4, Fridge discloses all of the claim elements / features as discussed above in rejection for claim 3 and incorporated herein by reference, but fails to disclose grouping combination of error shapes. Brecher (US pat no 5,544,256) discloses grouping to a combination of an area of error shape and a smallest linear dimension of the error shape (see fig 7 and col. 10 lines 3 – 5 – the circle shape defect is the smallest defect and is grouped with other shape errors). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include grouping to a combination of an area of error shape and a smallest linear dimension of the error shape because the smallest error shape are almost insignificant, so the grouping those smallest error shape with other shape groups save processing due to having to process less error shapes.

With regards to claim 19, see the rationale and rejection for claim 4.

4. Claims 5 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fridge (US pat no 4,648,053) in view of Chung (US pat no 5,481,472) as applied to claim 1 further in view of Bishop (US pat no 4,589,140).

With regards to claim 5, Fridge discloses all of the claim elements / features as discussed above in rejection for claim 3 and incorporated herein by reference, but fails to disclose forming one environment from expanded error shape. Bishop (US pat no 4,589,140) discloses expanding each error shape in the subset to form a corresponding expanded shape (see fig 7b – the defect shape is magnified or expanded) and form the at least one environment shape corresponding to each expanded shape by removing all portions of the expanded shape which are common to the second shape pattern (fig 7b is the environment shape; also the rest of the image, other than the defect area, in fig 7c are remove from to obtain the image in fig 7b). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include expanding the area of the defect because to obtain the detail shape of the defect in order to classify the defect, so it can be use later to identify defect shapes similar to the one being identify currently.

With regards to claim 20, see the rationale and rejection for clam 5.

6. Claims 6 – 10 and 21 – 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fridge (US pat no 4,648,053) in view of Chung (US pat no 5,481,472) as applied to claim 1 further in view of Simard (US pub no 2003/0202696).

With regards with claim 6, Fridge discloses all of the claim elements / features as discussed above in rejection for claim 1 and incorporated herein by reference, but fails to disclose outwardly projecting each bounding side of the error shape. Simard discloses a method of claim 5, wherein each error shape in the subset has a polygonal shape, and wherein expanding the first error shape comprises outwardly projecting each bounding side of the error shape by a distance in a direction perpendicular to the bounding side (see fig 3 to fig 4 – the objects in fig 3 is expanded into the objects in figure 4 – the distance of each side expanded is shown in fig 4 is two boxes perpendicular to the original shape for both shapes). It would have been obvious to one having ordinary skill in the art at the time of the invention to include expanding shape and forming at least one environment shape because to give a better view for user to identify the shapes for purpose of classification, as explained in the motivation for claim 2. Fridge and Simard are combinable because they are both in the field of detects detection.

With regards to claim 7 – 10, see the rejection and rationale for claim 6. In addition, the objects shown in figure four are in the same sub-set and both are

expanded by the same amount of size, which is two boxes perpendicular on each side of the polygon.

With regards to claim 21, see the rejection and rationale for claim 6.

With regards to claim 22, see the rejection and rationale for claim 7.

With regards to claim 23, see the rejection and rationale for claim 8.

With regards to claim 24, see the rejection and rationale for claim 9

With regards to claim 25, see the rejection and rationale for claim 10.

With regards to claim 16, see the rejection and rationale for claim 1

7. Claims 13 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fridge (US pat no 4,648,053) in view of Chung (US pat no 5,481,472) as applied to claim 1 further in view of Morrin ('411).

With regards with claim 13, Fridge discloses all of the claim elements / features as discussed above in rejection for claim 1 and incorporated herein by reference, but fails to disclose performing XOR on the first and second shape pattern. Morrin (US pat no

4,005,411) discloses obtaining a correlated error image by using exclusive OR operator (see col. 3 lines 66 – 67 to col. 4 lines 1 – 2).

It would have been obvious to one having ordinary skill in the art at the time of the invention to include XOR function because the output of an XOR function of two different values (when the defect detected on the image being inspected is outside the region of the original template when compared, values having 'OFF' XOR 'ON") is an 'ON' value indicting the position of the defect of the error shape, and distinguishing from regions that does not have errors (when two input values are the same 'OFF' XOR "OFF" or 'ON' XOR 'ON').

With regards to claim 28, see the rationale and rejection for claim 13.

8. Claims 15 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fridge ('053) in view of Chung ('472) as applied to claim 1 further in view of DeCamp (US pat no 6,063,132).

With regards to claim 15, Fridge discloses all of the claim elements / features as discussed above in rejection for claim 1 and incorporated herein by reference, but fails to disclose adding at least one anchor. DeCamp discloses a method of claim 1, wherein prior to the step of forming a first shape pattern the method further comprises providing a base geometry having at least one initial geometric shape (see fig 9 – 33 – as the initial geometric shape), and wherein the step of forming a first shape pattern comprises

adding at least one anchor to the at least one initial geometric shape (see fig 9 – 33G – is one of the anchors added to the initial geometric shape) such that the first shape pattern so formed includes the at least one initial shape and the at least one anchor so added (descriptions found on col. 6 lines 57 – 62). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include adding at least one anchor because to recognize the shape of the error shape, so the user or operator is able to classify the error shape for future reference.

With regards to claim 30, see the rationale and rejection for claim 15.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alex Liew whose telephone number is (571)272-8623. The examiner can normally be reached on 9:30AM - 7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso can be reached on (571)272-7695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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1/23/07